

21 a second interconnect selectively provided on the second interlayer
22 insulating film and electrically connected to the first interconnect through a second
23 contact hole formed in the second interlayer insulating film; and
24 a passivation layer provided so as to cover the second interconnect.

1 30. (Amended) A semiconductor device, comprising:

2 a capacitor provided on a supporting substrate having an integrated
3 circuit thereon and including a lower electrode, a dielectric film, and an upper
4 electrode, said dielectric film including a remnant polarization of approximately 10
5 $\mu\text{C}/\text{cm}^2$;

6 a first interlayer insulating film provided so as to directly cover the
7 capacitor;

8 a first interconnect selectively provided on the first interlayer
9 insulating film and electrically connected to the integrated circuit and the capacitor
10 through a first contact hole formed in the first interlayer insulating film;

11 a second interlayer insulating film having a tensile stress provided so
12 as to directly cover the first interconnect and the first interlayer insulating film;

13 a second interconnect selectively provided on the second interlayer
14 insulating film and electrically connected to the first interconnect through a second
15 contact hole formed in the second interlayer insulating film; and

16 a passivation layer provided so as to cover the second interconnect.

31. (Amended) A semiconductor device, comprising:

 a capacitor provided on a supporting substrate having an integrated
 circuit thereon and including a lower electrode, a dielectric film, and an upper
 electrode, said dielectric film including a remnant polarization of at least 10
 $\mu\text{C}/\text{cm}^2$;

 a first interlayer insulating film provided so as to directly cover the
 capacitor;

C2
a first interconnect selectively provided on the first interlayer insulating film and electrically connected to the integrated circuit and the capacitor through a first contact hole formed in the first interlayer insulating film;

a second interlayer insulating film having a tensile stress provided so as to directly cover the first interconnect and the first interlayer insulating film;

a second interconnect selectively provided on the second interlayer insulating film and electrically connected to the first interconnect through a second contact hole formed in the second interlayer insulating film; and

a passivation layer provided so as to cover the second interconnect.

Please cancel claim 2.

Please add claim 32.

C3
32 (Newly Added) A semiconductor device, comprising:

1 a capacitor provided on a supporting substrate having an integrated
2 circuit thereon and including a lower electrode, a dielectric film, and an upper
3 electrode;

5 a first interlayer insulating film provided so as to directly cover the
6 capacitor, the first interlayer insulating film having a tensile stress;

7 a first interconnect selectively provided on the first interlayer
8 insulating film and electrically connected to the integrated circuit and the capacitor
9 through a first contact hole formed in the first interlayer insulating film;

10 a second interlayer insulating film having a tensile stress provided so
11 as to directly cover the first interconnect and the first interlayer insulating film;

12 a second interconnect selectively provided on the second interlayer
13 insulating film and electrically connected to the first interconnect through a second
14 contact hole formed in the second interlayer insulating film, and

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a passivation layer provided so as to cover the second interconnect.